REMARKS

Claims 1 and 57 have been amended. Claims 29, 51, and 76 have been cancelled. No new claims have been added. Thus, claims 1-28, 30-50, and 52-77 are pending.

Claim 29, 51, and 76 stand rejected under 35 U.S.C. § 112, first paragraph, as allegedly being non-enabled. Claims 29, 51, and 76 have been cancelled.

Claims 1-27, 30-49, 52-75, and 77 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Halbert (U.S. Patent No. 6,625,687). Claims 28 and 50 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Halbert in view of Official Notice. These rejections are respectfully traversed.

Independent claim 1 recites:

> a selector circuit ... operating said first and second receiver and driver pairs ... such that in a first operating mode said first receiver and driver pair passes data between said first bus segment and an I/O device and bypasses said second bus segment, and in a second operating mode said first and second receiver and driver pairs pass data between respective adjacent bus segments and bypass said I/O device. (emphasis supplied)

Independent claims 9, 31 and 53 recite:

> an interface circuit coupled to said first and second receiver and driver pairs and a second data bus, wherein said interface circuit is configured to receive data from said first receiver and selectively place said data on said second data bus and receive data on said second data bus and selectively place said data on said first data bus. (emphasis supplied)

Independent claim 54 recites:

> wherein said at least one memory subsystem interface circuit includes first and second receiver and driver pairs connected to respective first and second segments of said bus, said first receiver and driver pair

> receiving data on said first segment using said first receiver and selectively placing data on said first segment using said first driver, and said second receiver and driver pair receiving data on said second segment using said second receiver and selectively placing data on said second segment using said second driver. (emphasis supplied)

Independent claim 57 recites:

> driving data using first and second drivers coupled to said respective first and second segments, said driving being performed according to a selection signal, such that in a first operating mode a first receiver and driver pair passes signals between said first segment of said first data bus and an I/O device and bypass said second segment, and in a second operating mode said first and a second receiver and driver pairs pass signals between respective adjacent bus segments and bypass said I/O device. (emphasis supplied)

Independent claim 60 recites: "selectively placing data received from said first bus segment on said second bus segment; selectively placing data received from said second bus segment on said first bus segment." (emphasis supplied)

Each of the above recited independent claim recites a method or apparatus in which a circuit is coupled to an I/O device, a first segment of a first bus, and a second segment of a first bus. Additionally, the circuit which is operable in a first mode wherein data is transmitted between the first segment of the first bus and the I/O device while bypassing the second segment of the first bus, or a second mode wherein data is transmitted between the first and second segments of the first bus while bypassing the I/O device. Alternatively phrased, the apparatus and method selectively places data between a first bus segment and a second bus segment of a first data bus. Limitations appearing in the above recited portions of the independent claim is consistent with a straight (i.e., non-ring) bus topology as described in the application. See, e.g., Fig. 1.

In contrast Halbert discloses a ring-bus system. See, e.g., Fig. 4, at bus 320. Halbert further discloses the use of junction circuits (e.g., Fig. 4, circuit 312a, circuit 312b; Fig. 5, circuit 500). The junction circuits of Halbert couple between a first and a second bus segment of the ring bus 320, and to another bus (e.g., Fig. 5, bus 502).

However, Halbert fails to disclose or suggest the above recited limitations of the independent claims due to the use of a ring bus topology. More specifically, Halbert discloses at column 2, lines 9-20:

> [A] memory module includes at least one memory device and a junction circuit. The junction circuit has a first port to couple to a bus from alternatively a memory controller and a daisy-chained other memory module. The junction circuits [sic] has a second port coupled to the memory devices, and a third port coupled to a bus from alternatively a memory controller or a daisy chained other memory module. The junction circuit sends data received from the first port to the second port and the third port, sends data received from the second port to the first port and the third port, and sends data received from the third port to the second port and the first port.

Thus, Halbert discloses a junction circuit which always rebroadcasts data received on any one of three ports to the two remaining other ports. Thus, Halbert fails to disclose or suggest "bypassing" either an I/O device or a second segment of a data bus as required by independent claims 1 and 57. Similarly, Halbert fails to disclose or suggest "selectively placing data" as required by independent claims 9, 31, 53, 54, and 60.

Accordingly, independent claims 1, 9, 31, 53, 54, 57, and 60 are believed to be allowable over the prior art of record. Depending claims 2-8, 10-28, 30, 32-50, 52, 55-56, 58-59, 61-77 are also believed to be allowable for at least the same reasons as the independent claims.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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